

OPEN-SOURCE XILINX FPGA POWERLINK PACKAGE

Benjamin VENDITTI, Research Engineer
AIT \ VAC \ High-Performance Vision Systems



WHAT IS CDI2 ? - MAIN GOALS

CDI = Common Detector Interface

CDI2 specifies the interfaces (mechanic, electronic, communication and data) between a sensor (camera, or any other sensor) and a banknote sorting machine with the following goals

- Enables *integration* of 3rd party Camera System and Sensors into Banknote Sorting Machines (BSM)
- Enables *new ways* of sensors development independent from the BSM
- Defines *sensor fusion* capabilities to share data and results from different sensors
- Provides *new opportunities* to enhance note processing in banknote sorting
- Promotes *global standardization* and enhanced note analysis

CDI2 is a joint development of the Eurosystem and the US Federal Reserve

CDI2 - CAMERA SYSTEM, EVALUATION UNIT & DETECTOR

Camera System

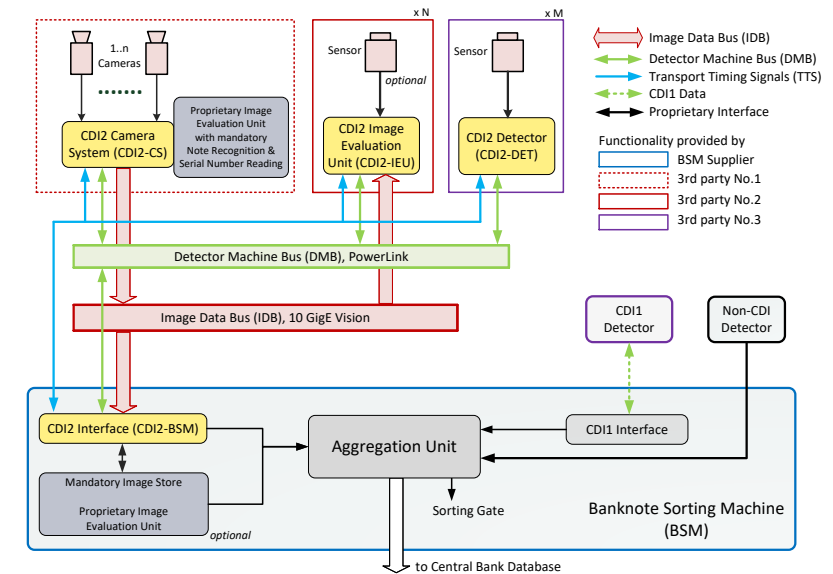
Set of multiple cameras, installed at a belt free area position of the BSM. Delivers the images of the banknotes to the Image Data Bus.

Image Evaluation Unit

A device evaluating images delivered from the Camera System. It may be integrated in the Camera System itself or can collect and evaluate images from the Image Data Bus. Optionally these data can be combined with own sensor data.

Detector

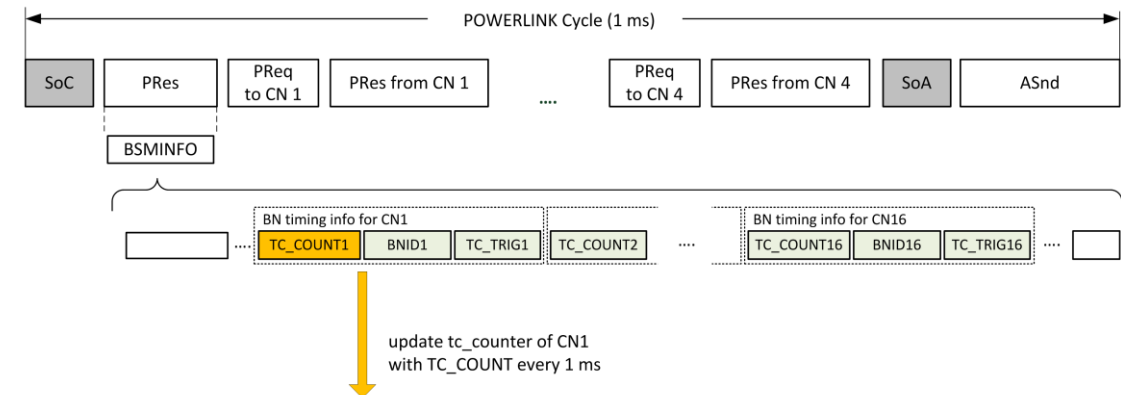
A device for inspecting banknotes for authentication or specific features on a BSM (e.g. magnetism).



CDI2-POWERLINK CHALLENGES

CDI2 has 3 hard real-time requirements

- CN Poll reaction time
- CN need to generate BN present signal from BSMINFO frame (without TTS)
- Async PowerLink Communication
TCP/IP packaging and reaction time



CDI2.7D Specification, Page 54, Figure 21: Readout of TC_COUNTn from BNINFO

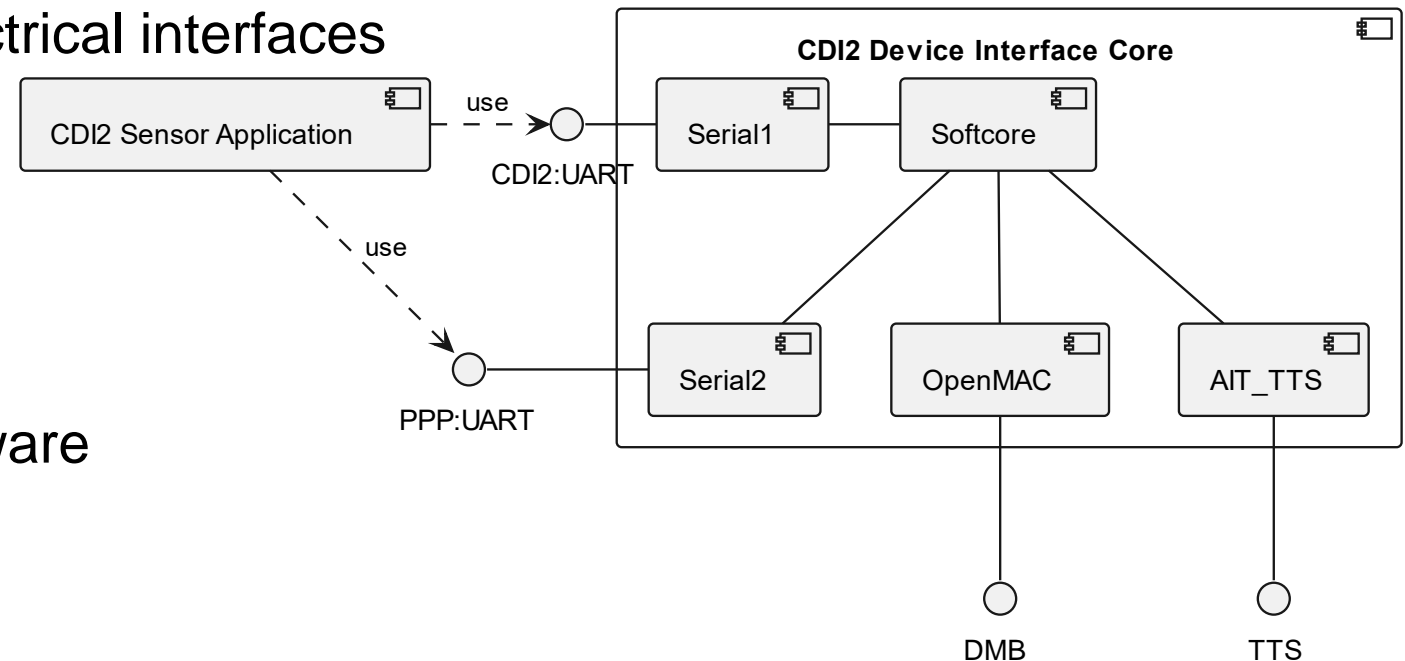
Item	Value	Unit	Note
POWERLINK cycle time	1000	µs	D_NMT_CycleTimeMax_U32 D_NMT_CycleTimeMin_U32
PReq to PRes latency (CN)	10	µs	CN isochronous reaction time
SoA to ASnd latency (CN)	25	µs	CN asynchronous reaction time

CDI2.7D Specification, Page 128, Excerpt of Table 46: POWERLINK device data sheet, displaying critical device properties

OPEN-SOURCE XILINX FPGA POWERLINK PACKAGE

Key Benefits for Suppliers

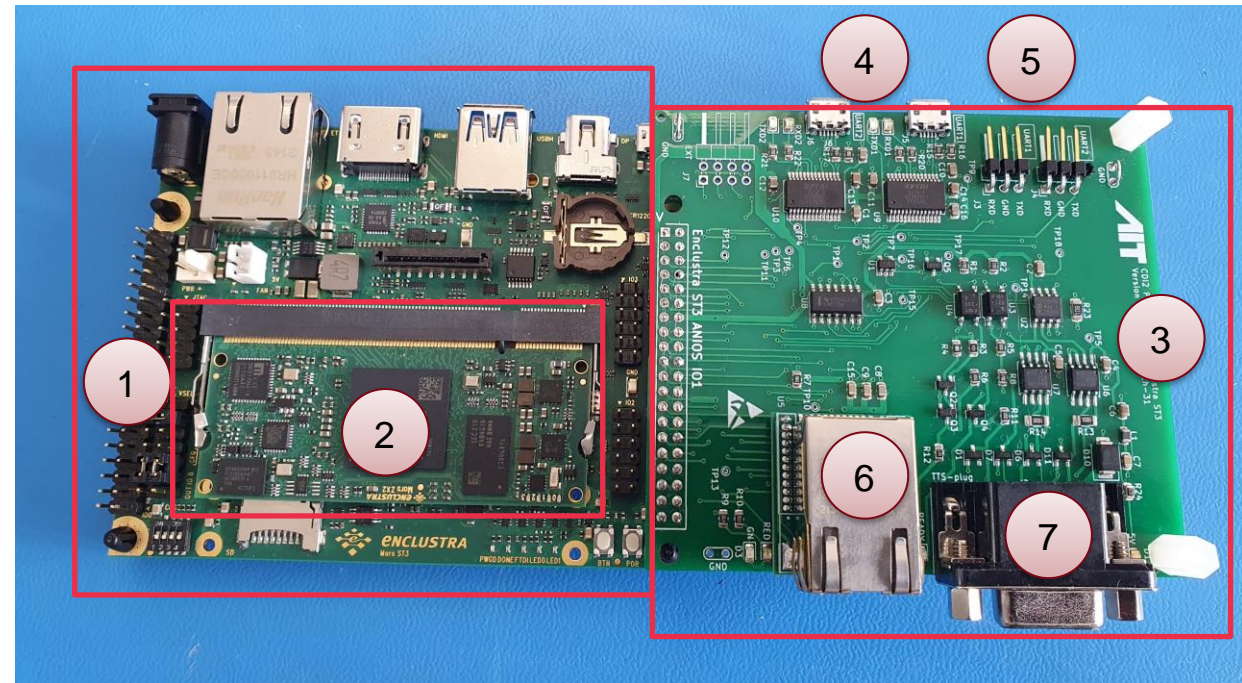
- Simplifies connection of a sensor to a CDI2 compliant BSM
- Uses FPGA middleware to meet real-time requirements
- Provides all CDI2 mandatory electrical interfaces
- Hides Powerlink complexity
- Provides simple serial command interface for easy integration
- Build from readily available hardware



HARDWARE OVERVIEW

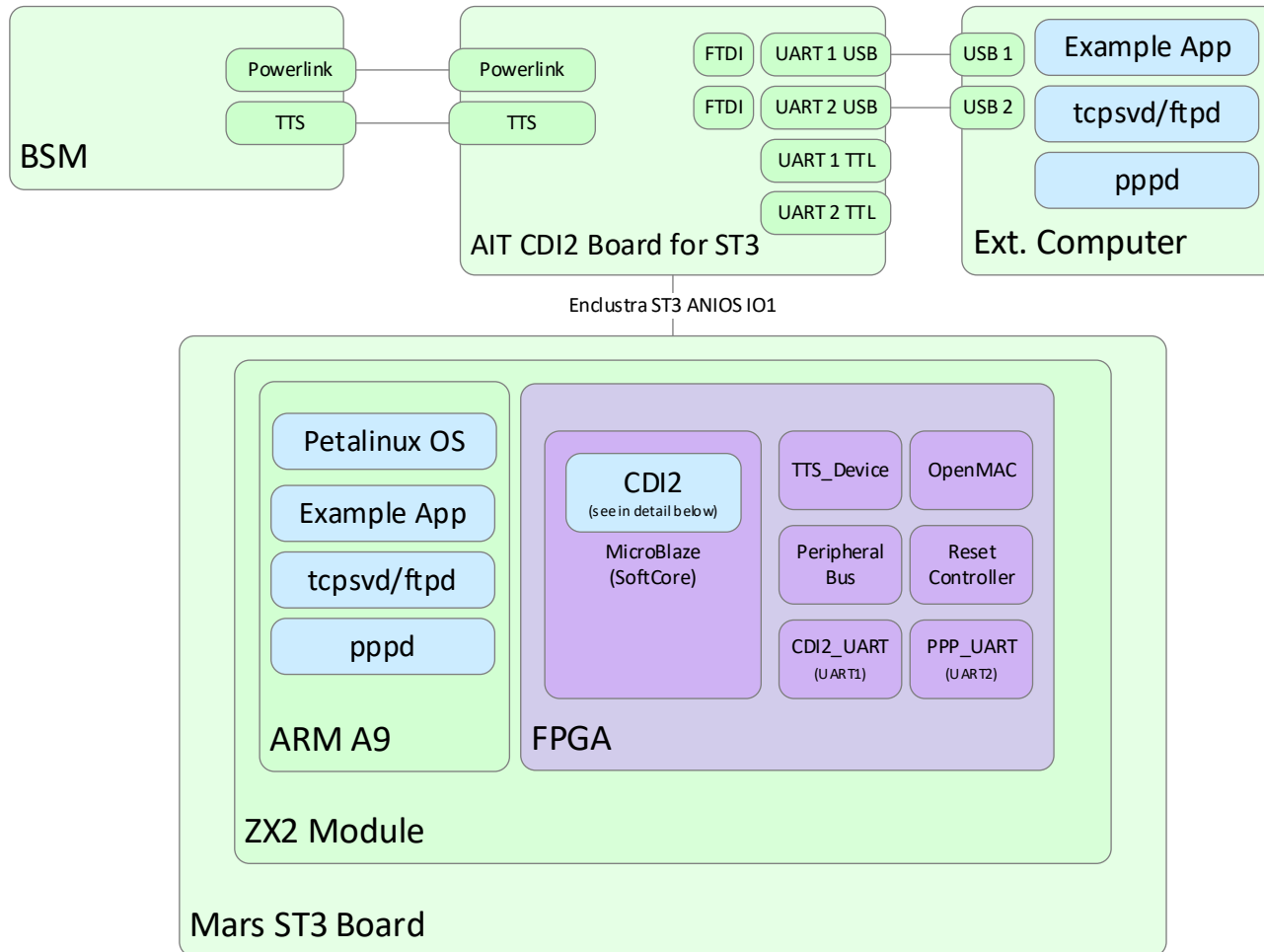
1. Enclustra Mars ST3 Base Board
2. Enclustra Mars ZX2 SoC Module
3. AIT CDI2 Board for ST3 v1.1
4. USB UART1/2
5. TTL UART 1/2
6. DMB (PowerLink) Port
7. TTS Port

Boots from SD Card or QSPI



Hardware modules of the Simplified CDI2 Device

ARCHITECTURE OVERVIEW



Hardware

FPGA

Software

- OpenMAC IP Core by B&R supporting real-time req. of PowerLink
- AIT TTS IP Core
- AIT CDI2 Core running on MicroBlaze
- Standard Xilinx IP Cores
- AIT CDI2 device application on
 - Internal ARM A9 dual-core
 - Or external computer

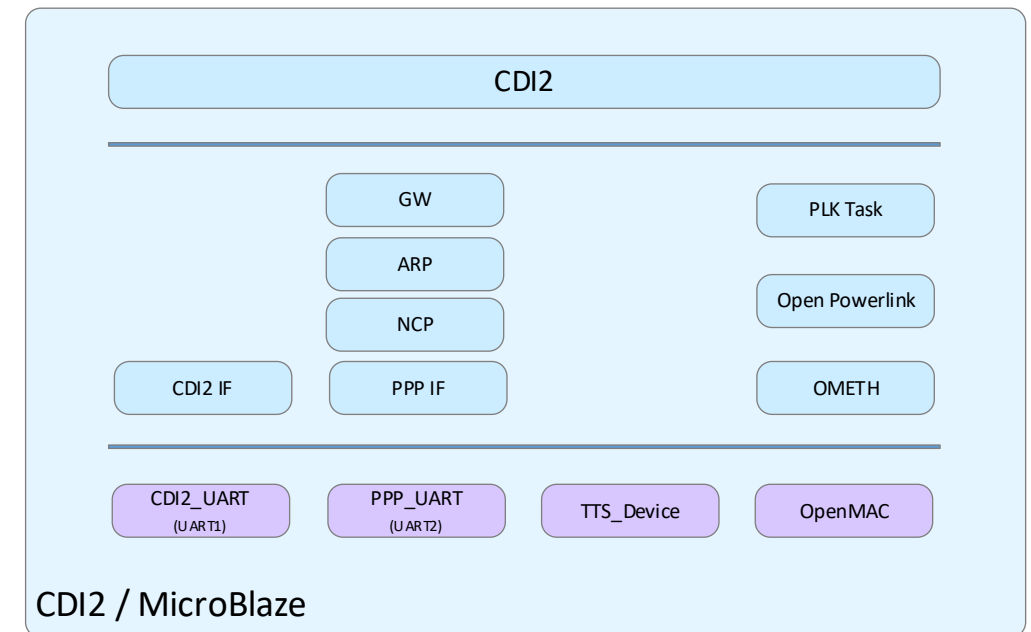
CDI2 CORE / MICROBLAZE

- FreeRTOS with Xilinx BSP
- PowerLink Layer based on OpenPowerLink (B&R)
- Implements PowerLink Node Management state machine
- PowerLink PPP Gateway and ARP
- Handles hard real-time requirements of PowerLink & CDI2
- Implements CDI2 Serial IF
- All modules written in C

Hardware

FPGA

Software



SERIAL PROTOCOL OVERVIEW

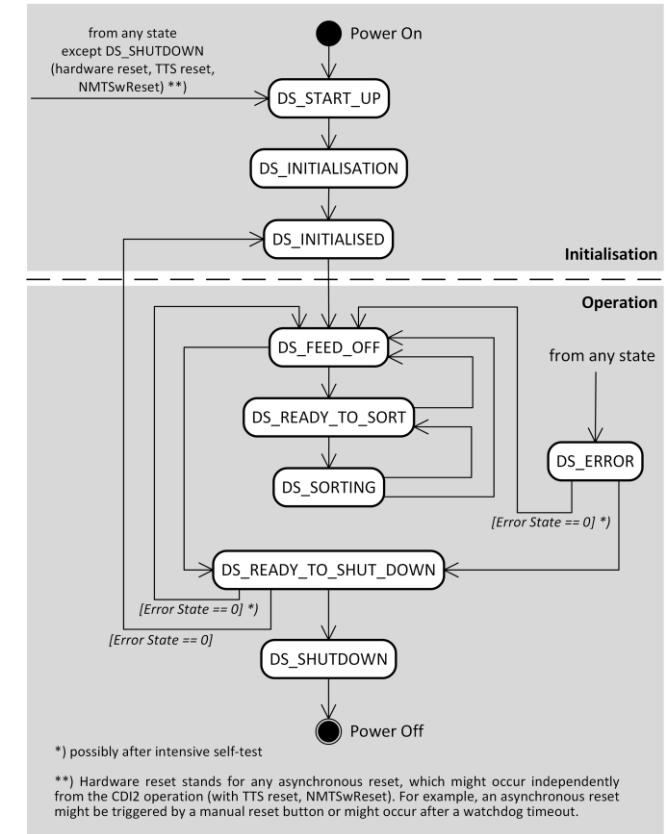
Command/Response ID	Full Name	Direction	Length	Operation Phase
0x10	Software Detector Reset	App→Core	6	Startup
0x11	Protocol Version	App→Core	7	
0x21	Protocol Version Answer	Core→App	13	
0x12	Machine Info (reserved)			
0x22	Detector Info (reserved)			
0x23	TTS Reset	Core→App	5	
0x24	NMT Reset	Core→App	6	
0x15	Start CDI2	App→Core	8	
0x25	Start CDI2 Answer	Core→App	5	
0x16	DET Status	App→Core	6	
0x26	BSM Status	Core→App	6	
0x17	Set Maintenance State	App→Core	6	
0x18	Set Error State	App→Core	6	
0x29	FATAL	Core→App	6+N	
0x2A	ERROR	Core→App	6+N	
0x2B	WARNING	Core→App	6+N	
0x2C	INFO	Core→App	6+N	
0x2D	DEBUG	Core→App	6+N	
0x2E	TRACE	Core→App	6+N	
0x80	Banknote Trigger	Core→App	10	Sorting
0x81	Banknote ID	Core→App	21	
0x82	Banknote Info	Core→App	12	
0x83	Banknote ID and Info (reserved)			
0x41	Banknote Result	App→Core	13+N	
0x42	Banknote Recognition	App→Core	12	
0x84	Feed Off (reserved)			
0x44	Feed Off Answer (reserved)			
0x85	Feed On (reserved)			
0x45	Feed On Answer (reserved)			
0x86	Raw Data Request (reserved)			Feed Off
0x46	Raw Data Answer (reserved)			
0x47	Accept Update	App→Core	5	
0x48	Reject Update	App→Core	5	
0x87	Prepare Update	Core→App	5	
0x88	Perform Update	Core→App	5	

EXAMPLE SENSOR APPLICATION

- Blueprint for hardware suppliers
- Implements the CDI2 device state-machine
- Can act as detector or camera system
- Written in python, bash
- Accompanied by all relevant services - *pppd*, *httpd*, *ftpd*
- Runs on Ubuntu 22.04 LTS and PetaLinux

```

CDI2_DeviceApp:~/App$ sudo ./cdi2app.sh -help
usage: ./cdi2app.sh [-r|--role arg] [-i|--nodeId arg] [-d|device arg] [-s|--resultSize arg] [-l|--log arg] [--help] [--noTTS]
-r, --role           Set the cdi2 device role [Camera|Detector]
-i, --nodeId         Set the cdi2 device node id [1,16], default is 1/2 depending on the role Camera/Detector.
-d, --device         Set the uart devices to use, default is '/dev/ttyS0,/dev/ttyS1'
-s, --resultSize     Set the size of the BnResult [15,1412] being sent.
-l, --log            Set the log level [DEBUG, INFO, WARNING, ERROR, CRITICAL], default is 'INFO'.
--noTTS             Disable TTS
--help              Prints this description.
  
```



CDI2.7D Specification, Page 69
 Figure 32: CDI2 Device states and transitions

THE OPEN-SOURCE XILINX FPGA POWERLINK PACKAGE

- CDI2/PowerLink implementation provided as drag & drop Xilinx IP Core
- Schematics for AIT CDI2 Board for ST3 v1.1 extension board
- Includes example application implementation (detector, camera) with source code
- Includes FPGA design sources
- Includes API description and documentation
- Successfully tested with BSMS, *test on M8 follows soon*
- Soon available for download from the ECB website

THANK YOU!

Benjamin Venditti

Research Engineer

benjamin.venditti@ait.ac.at

Phone: +43 664 8251168





WIRESHARK PL/CDI2 STATISTICS

Wireshark · Powerlink Timing Statistics

Total Powerlink packet count: 49549

- SoC - time delta between SoC
Count, Min, max, avg, sd [ms]: 12876, 0,999995, 1,000000, 0,999998, 0,000002
- PReq - time delta since SoC
Count: 3207
Dest. node 1, count, min, max, avg, sd [ms]: 3207, 0,032235, 0,032245, 0,032240, 0,000001
- PRes - time delta since SoC for MN or PReq(node)
Count: 16082
Managing node, count, min, max, avg, sd [ms]: 12876, 0,011755, 0,011765, 0,011760, 0,000001
Src. node 1, count, min, max, avg, sd [ms]: 3206, 0,008945, 0,009065, 0,009011, 0,000026
- SoA - time delta since SoC
Count, min, max, avg, sd [ms]: 16932, 0,032235, 0,186160, 0,070567, 0,066561
- ASnd - time delta since SoA
Count: 452
Managing node, count, min, max, avg, sd [ms]: 25, 0,006720, 0,012480, 0,006950, 0,001129
Src. node 1, count, min, max, avg, sd [ms]: 13, 0,009010, 0,009020, 0,009017, 0,000003
Src. node 32, count, min, max, avg, sd [ms]: 414, 0,011290, 0,011565, 0,011495, 0,000032

Hervorgehoben:

Schließen

- Tested with BSM Simulator @ 50BNs/sec, w/o TS
- Sorting Test Run of 1000 BNs
- BNResult Size = 256 byte

Wireshark · CDI2 Timing Statistics

Detected nodes: 1:CS, 240:BSM

Packet counts

Packet Type	Node	Type	Count	BNINFOs	BNRECs	TC_TRIGs	Res.Segs	Results
BNRESULTReq	240	BSM	5227	0	0	0	0	0
BNRESULT	1	CS	5226	0	1000	0	1000	1000
BSMINFO	240	BSM	20951	1000	0	1000	0	0
All	All		31404	1000	1000	1000	1000	1000

Encountered banknote IDs

From ID	Till ID	Count
1	1000	1000

Timing

Statistics-Type	Node	Type	Count	Min [ms]	Max [ms]	Average [ms]	St.Dev. [ms]
TC_TRIG to trigger delay	1	CS	1000	14,999955	16,999970	15,008970	0,104494
Trigger to BNREC delay			1000	8,029405	8,029535	8,029475	0,000026
BNREC to BNINFO delay			1000	2,970445	2,970570	2,970503	0,000026
Trigger to 1st result seg. delay	1	CS	1000	24,029365	28,029400	24,033442	0,126427

Hervorgehoben:

Schließen